Jc976 U.S. PTO
09/917127
07/27/01

Subclass	Class	ISSUE CLASSIFICATION

U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE
FA 2823 AC	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/917127	D	~~257~~ 438	612	~~2815~~ 2822	Smith

APPLICANTS: Larry Kinsman
Salman Akram

TITLE: Method for fabricating a chip scale package using wafer level processing and devices resulting therefrom

PTO-2040
12/99

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ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)							
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)						
INTERNATIONAL CLASSIFICATION									
			☐ Continued on Issue Slip Inside File Jacket						

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☐ The term of this patent subsequent to _____ (date) has been disclaimed.

☐ The term of this patent shall not extend beyond the expiration date of U.S. Patent No. _____

☐ The terminal ___ months of this patent have been disclaimed.

DRAWINGS			CLAIMS ALLOWED	
Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.

(Assistant Examiner) (Date)

(Primary Examiner) (Date)

(Legal Instruments Examiner) (Date)

NOTICE OF ALLOWANCE MAILED

ISSUE FEE

Amount Due	Date Paid

ISSUE BATCH NUMBER

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